



IT1167E

High Speed 2 Channel USB2.0 Flash Controller

Preliminary Specification V0.2

ITE TECH. INC.



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Revision History

Section	Revision	Page No.
-	Initial Release	-
All	Revise version number	-
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1. Features

■ Spec Compliance

- High speed USB2.0 interface
- Backward compatible to USB1.1
- Integrated USB2.0 Transceiver Macrocell Interface (UTMI) and Serial Interface Engine (SIE)

ISP

Support firmware ISP function to upgrade firmware

■ Enhanced Hardware Monitor

- Support 2 flash access channels
- Support up to 16 flash connection
- Support advanced ECC algorithm from 14 bit per 512B to 30 bit per 1KB hardware BCH ECC

■ Flash Support

- Support SLC/MLC flash
- Support 2K byte/page, 4K byte/page and 8K byte/page flash architecture with multi-channel support
- Support 2 plane operation
- Support Samsung / Hynix / Intel / Micron / PFC / Toshiba / STM flash / SMIC latest flash spec.
- Support interleave mode to accelerate read/write performance
- Support ONFI2.0 flash spec. & DDR mode access
- Support 1.8/3.3V flash

■ Multi Partition with Proprietary Tool

- One Read-Only partition is designated for Auto-Run feature
- One or two public partitions with or without security partition
- One public partition plus Auto-Run feature with or without security partition
- Security partition can be protected by password
- Capacity configuration of each partition can be done while factory initialization or by accompanied utility
- Hardware Write-Protect Switch for Security Purpose
- Integrated 5V to 3.3V/1.8V voltage regulator to provide 3.3V for pad and 1.8 V for core operation
- Customized VID/PID and Serial Number
- Windows 7/Windows 98SE/ME/2000/XP/Vista, Mac 9.x above and Linux kernel 2.4 above Compatible
- LED indicator to show three different access status, Busy, Waiting, and Off

■ Package

1

LQFP 64/48 pin





2. General Description

IT1167 leverages the state-of-art flash control technology to achieve extremely high performance with all types of flash technology with the 2 independent flash access channel design. With 2 independent channels, not only general read/programming performance maximizes USB2.0 bandwidth but also provides the cutting-edge flash bad block management without suffering capacity lost due to high bad blocks count.

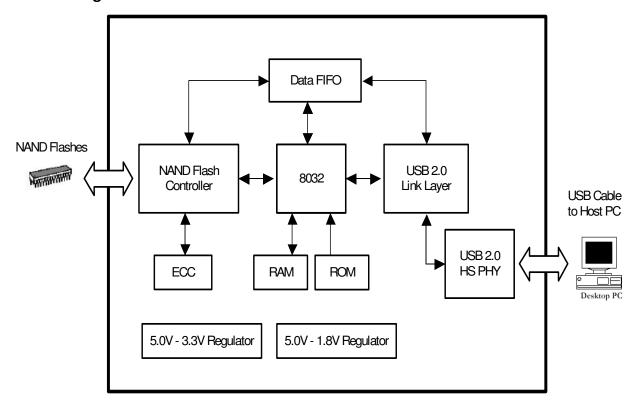
As a legacy tradition from iTE flash controllers, IT1167 broadens customers' flash selection by its industry-leading 30 bit hardware ECC engine, which remains customers more competitive on latest flash technology, including Hynix 32nm/Samsung 35nm/IM 34nm/Toshiba 43nm or more advanced parts, either SLC, MLC or TLC specification. Further more, IT1167 completes ONFI2.0 design on DDR type flash support to create end product difference in terms of performance and reliability.

Differed from previous generic designs, propelling new flash interleave algorithm and flash management with efficiency-oriented independent channel design on firmware architecture, that IT1167 sets up a new challenging mantra to last generation products.





3. Block Diagram







4. Pin Configuration

Figure 4-1 LQFP 64 Pin Configuration

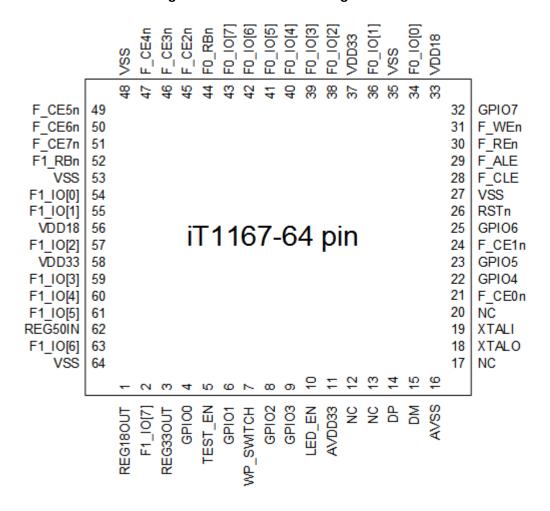
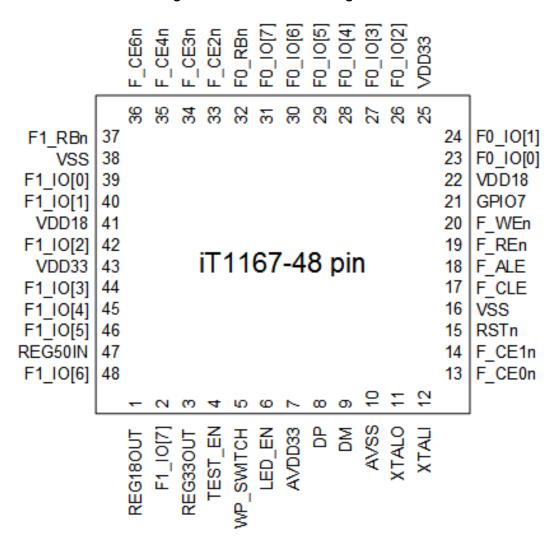




Figure 4-2 LQFP 48 Pin Configuration









5. Pin Description

Table 5-1 LQFP 64 Pin Description

Pin. ₁	Signal. ₁	Attribute.	Description.	Pin.	Signal. ₁	Attribute.1	Description.
1.5	REG18OUT.,	P.	Regulator 1.8V Power Out Connect External Capacitor (10 0.1 uF) to Ground).	33.,	VDD18.,	P.a	Logic 1.8V Power.,
2.1	F1_IO[7].	I/O. ₁	Group 1 Flash Data Bus - bit 7 or GPIO Bus - Port 1 bit 7.	34.1	F0_IO[0].,	I/O.,	Group 0 Flash Data Bus - bit 0.
3.1	REG33OUT.	P.a	Regulator 3.3V Power Out (Connect External Capacitor (10 0.1 uF) to Ground).	35.1	VSS.,	P.a	Logic Ground.
4.1	GPIO0.1	I/O. ₁	GPIO Bus – Port 3 bit 0.,	36.1	F0_IO[1].,	I/O. ₁	Group 0 Flash Data Bus - bit 1.
5.1	TEST_EN. ₁	La	Test Mode Enable Pin.	37.1	VDD33.1	P.,	Logic 3.3V Power.
6.1	GPIO1.1	I/O. ₁	GPIO Bus – Port 3 bit 1.1	38.1	F0_IO[2].,	I/O. ₁	Group 0 Flash Data Bus - bit 2.1
7.,	WP_SWITCH.	La	Write Protect Switch Input (active low).	39.,	F0_IO[3].,	I/O.1	Group 0 Flash Data Bus - bit 3.,
8.1	GPIO2.1	I/O.1	GPIO Bus – Port 3 bit 2.1	40.1	F0_IO[4].1	I/O.1	Group 0 Flash Data Bus - bit 4.1
9.1	GPIO3.1	I/O.1	GPIO Bus - Port 3 bit 3.1	41.1	F0_IO[5].1	I/O.1	Group 0 Flash Data Bus - bit 5.1
10.1	LED_EN. ₁	O. ₁	LED Indication.	42.1	F0_IO[6].1	I/O.1	Group 0 Flash Data Bus - bit 6.1
11 .a	AVDD33.1	P. ₁	Analog 3.3V Power.	43.1	F0_IO[7].,	I/O.1	Group 0 Flash Data Bus - bit 7.1
12.1	NC.1	1	NC.,	44.1	F0_RBn.₁	La	Group 0 Flash Ready_Busy (active low).
13.,	NC.1	1	NC.,	45.1	F_CE2n. ₁	O.1	Flash Chip Enable - Chip 2 (active low).
14.1	DP.1	I/O.1	USB Data Positive Pin.,	46.1	F_CE3n. ₁	O.1	Flash Chip Enable - Chip 3 (active low).
15.,	DM.,	I/O.1	USB Data Negative Pin.,	47 .1	F_CE4n.,	O.1	Flash Chip Enable - Chip 4 (active low).
16.1	AVSS.1	Pa	Analog Ground.	48.1	VSS. ₁	Pa	Logic Ground.
17 .a	NC.	1	NC.1	49.1	F_CE5n. ₁	0.1	Flash Chip Enable - Chip 5 (active low).
18.,	XTALO.,	O.1	Crystal Output.	50 .1	F_CE6n.,	0.1	Flash Chip Enable - Chip 6 (active low).
19.1	XTALI.1	La	Crystal Input (12 MHz).,	51 .a	F_CE7n. ₁	0.1	Flash Chip Enable - Chip 7 (active low).
20.1	NC.1	1	NC.1	52.1	F1_RBn. ₁	La	Group 1 Flash Ready_Busy (active low).



21.1	F_CE0n.	O.,	Flash Chip Enable - Chip 0 (active low).	53.,	VSS.1	P.	Logic Ground.
22.1	GPIO4.1	I/O. ₁	GPIO Bus – Port3 bit 4.,	54.1	F1_IO[0]	1/0.1	Group 1 Flash Data Bus - bit 0 or GPIO Bus - Port 1 bit 0
23.1	GPIO5.,	I/O.1	GPIO Bus – Port 3 bit 5.1	55.,	F1_IO[1].,	I/O. ₁	Group 1 Flash Data Bus - bit 1 or GPIO Bus - Port 1 bit 1
24.1	F_CE1n.	O.1	Flash Chip Enable - Chip 1 (active low).	56.1	VDD18.1	P.a	Logic 1.8V Power .1
25.1	GPIO6.,	1/0.1	GPIO Bus – Port 3 bit 6.,	57.1	F1_IO[2].,	1/0.1	Group 1 Flash Data Bus - bit 2 or GPIO Bus - Port 1 bit 2
26.1	F_WPn., RSTn.,	On a a In	Flash Write Protect (active Iow) External Reset Pin (active Iow).	58.1	VDD33.,	P.,	Logic 3.3V Power .1
27.1	VSS.	P.,	Logic Ground.	59.1	F1_IO[3].,	I/O. ₁	Group 1 Flash Data Bus - bit 3 or GPIO Bus - Port 1 bit 3.
28.1	F_CLE.	O.1	Flash Command Latch Enable.	60.1	F1_IO[4].	I/O. ₁	Group 1 Flash Data Bus - bit 4 or GPIO Bus - Port 1 bit 4.
29.1	F_ALE.	O.1	Flash Address Latch Enable.	61.1	F1_IO[5].,	I/O. ₁	Group 1 Flash Data Bus - bit 5 or GPIO Bus - Port 1 bit 5
30.1	F_REn.,	O.1	Flash Read Enable (active low).	62.1	REG50I.N.	P _a	Regulator 5.0V Power In .
31.1	F_WEn.	0.1	Flash Write Enable (active low).	63.1	F1_IO[6].,	1/0.1	Group 1 Flash Data Bus - bit 6 or GPIO Bus - Port 1 bit 6.
32.1	GPI07.1	I/O.1	GPIO Bus – Port 3 bit 7.	64.1	VSS.1	P.s	Logic Ground .

*I: input, O: output, IO: bi-direction, P: power



Table 5-2 LQFP 48 Pin Description

Pin.	Signal.	Attribute.	Description.	Pin.	Signal. ₁	Attribute.	Description.
1.5	REG18OUT.,	Pa	Regulator 1.8V Power Out (Connect External Capacitor (10 0.1 uF) to Ground).	25.1	VDD33.,	P.,	Logic 3.3V Power.
2.1	F1_IO[7].	I/O.1	Group 1 Flash Data Bus - bit 7.	26.1	F0_IO[2].,	I/O.1	Group 0 Flash Data Bus - bit 2.1
3.1	REG33OUT.	P _a	Regulator 3.3V Power Out.	27 .1	F0_IO[3].,	I/O. ₁	Group 0 Flash Data Bus - bit 3.
4.1	TEST_EN.	La	Test Mode Enable Pin.	28.,	F0_IO[4].,	I/O. ₁	Group 0 Flash Data Bus - bit 4.1
5.1	WP_SWITCH.	La	Write Protect Switch Input (active low).	29.1	F0_IO[5].,	I/O.1	Group 0 Flash Data Bus - bit 5.1
6.1	LED_EN.	O.1	LED Indication.	30.1	F0_IO[6].,	I/O.1	Group 0 Flash Data Bus - bit 6.1
7 .1	AVDD33.1	P.a	Analog 3.3V Power.	31.	F0_IO[7].,	I/O. ₁	Group 0 Flash Data Bus - bit 7.
8.1	DP.1	I/O.1	USB Data Positive Pin.,	32.1	F0_RBn.₁	La	Group 0 Flash Ready_Busy (active low).
9.1	DM.	I/O.,	USB Data Negative Pin.,	33.1	F_CE2n.,	0.1	Flash Chip Enable - Chip 2 (active low).
10.1	AVSS.,	P.,	Analog Ground.	34.1	F_CE3n.,	O.a	Flash Chip Enable - Chip 3 (active low).
11 .a	XTALO.,	O.,	Crystal Output.	35.1	F_CE4n.,	O.a	Flash Chip Enable - Chip 4 (active low).
12.1	XTALI.1	La	Crystal Input (12 MHz).,	36.1	F_CE6n.,	O.a	Flash Chip Enable - Chip 6 (active low).
13.1	F_CE0n.	O. ₁	Flash Chip Enable - Chip 0 (active low).,	37.1	F1_RBn.,	La	Group 1 Flash Ready_Busy (active low).
14.1	F_CE1n.	O. ₁	Flash Chip Enable - Chip 1 (active low).	38.1	VSS.,	P.a	Logic Ground.
15.,	E_WPn+	O.i	Flash Write Protect (active low) External Reset Pin (active low)	39.1	F1_IO[0].,	I/O.,	Group 1 Flash Data Bus - bit 0.
16.1	VSS.1	Pa	Logic Ground.	40.1	F1_IO[1].	I/O.1	Group 1 Flash Data Bus - bit 1.
17.1	F_CLE.	O.1	Flash Command Latch Enable.	41.1	VDD18.1	Pa	Logic 1.8V Power.
18.,	F_ALE.	O.1	Flash Address Latch Enable.	42.1	F1_IO[2].,	I/O. ₁	Group 1 Flash Data Bus - bit 2.
19.1	ELRED.	O. ₁	Flash Read Enable (active low).,	43.1	VDD33.1	P.a	Logic 3.3V Power.
20.1	EWEn.	O.1	Flash Write Enable (active Iow).,	44.1	F1_IO[3].,	I/O. ₁	Group 1 Flash Data Bus - bit 3.
21.1	GPI07.1	I/O.1	GPIO Bus – Port 3	45.1	F1_IO[4].	I/O.1	Group 1 Flash



			bit 7.1				Data Bus - bit 4.1
22.1	VDD18.1	P.,	Logic 1.8V Power.	46.1	F1_IO[5].,	I/O.1	Group 1 Flash Data Bus - bit 5.1
23.1	F0_IO[0].1	I/O.1	Group 0 Flash Data Bus - bit 0.	47.,	REG50).N.,	P.,	Regulator 5.0V Power In.
24.1	F0_IO[1]. ₁	I/O.1	Group 0 Flash Data Bus - bit 1.	48.1	F1_IO[6].	I/O.1	Group 1 Flash Data Bus - bit 6.1

*I: input, O: output, IO: bi-direction, P: power



6. DC Characteristics

Absolute Maximum Ratings

Storage Temperature (Tstorage)_____-40°C to 85°C Ambient Operating Temperature (Ta)____0°C to 75°C

Comments

Extended exposure to the maximum ratings might degrade device reliability. Although IT1167 has protective circuitry to resist damage from electrostatic discharge (ESD), precautions should always be taken to avoid high voltage or electric field.

Table 6-1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit	Note
T _{storage}	Storage Temperature	-40	85	∞	-
Та	Ambient Operating Temperature	0	75	°C	-
REG33V	3.3V Supply Voltage	-0.3	3.6	V	-
REG18V	1.8V Supply Voltage	-0.3	2	٧	-
VDD33	3.3V Buffer Input Voltage	-0.3	3.6	V	-
REG5V	3.3V/5V Buffer Input Voltage	-0.3	5.5	V	-
IOVDD with 3.3V	3.3V Buffer Input Voltage	-0.3	3.6	V	
IOVDD with 1.8V	1.8V Buffer Input Voltage	-0.3	2	V	-

Table 6-2 Operating Conditions

Symbol	Parameter		Max.	Unit
REG5V	USB 5V Supply Voltage	3.2	5.5	V
REG33V	3.3V Supply Voltage		3.6	V
REG18V	1.8V Supply Voltage	1.6	2	V

Table 6-3 DC Characteristics of I/O Interface

Symbol	Parameter	Min	Max	Unit
V _{IH_TTL}	TTL Input High Voltage	2	VDD33+0.3	V
V _{IL_TTL}	TTL Input Low Voltage	-0.3	0.8	V
V _{OH_TTL}	TTL Output High Voltage	0.9VDD33		V
V _{OL_TTL}	TTL Output Low Voltage		0.45	V
I _{OH_TTL}	TTL Output High Current	-4		mA

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Symbol	Parameter		Max	Unit
I _{OL_TTL}	TTL Output Low Current		4	mA
V _{IH_USB}	USB Input High Voltage for Low-/full-speed	2.0		V
V _{IL_USB}	USB Input Low Voltage for Low-/full-speed		0.8	V
V _{I_USB_DIFF}	Differential Input Sensitivity for Low-/full-speed	TBD		V
V _{I_USB_CM}	Differential Common Mode Input Range for Low-/full-speed	8.0	2.5	V
V _{I_USB_HSSQ}	USB High-speed squelch Input detection threshold	0.1	0.15	V
V _{I_USB_HSDSC}	_usb_Hsdsc		0.625	V
V _{I_USB_HSCM}	USB High-speed Signaling Common Mode Range	-0.05	0.5	V
V _{OH_USB}	USB Output High Voltage for Low-/full-speed	2.8	3.6	V
V _{OL_USB}	USB Output Low Voltage for Low-/full-speed	0	0.3	V
V _{OH_USB_HS}	USB Output High Voltage for High-speed	0.36	0.44	V
V _{OL_USB_HS}	USB Output Low Voltage for High-speed	-0.01	0.01	V
I _{OH_USB}	USB Output High Current for Low-/full-speed	-10		mA
I _{OL_USB}	I _{OL_USB} USB Output Low Current for Low-/full-speed		10	mA
I _{OH_USB_HS}	USB Output High Current for High-speed	-40		mA
lol_usb_hs	USB Output Low Current for High-speed		40	mA



7. AC Characteristics

Table 7-1 AC Characteristics

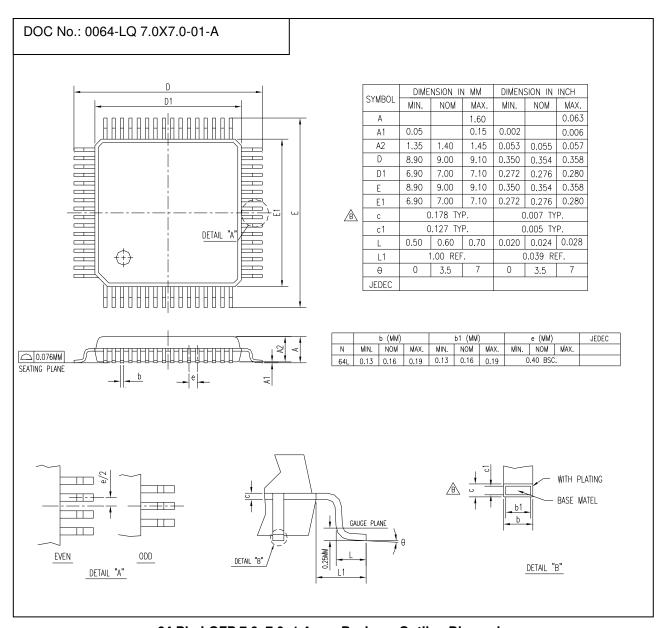
Symbol	Parameter	Min.	Тур.	Max.	Unit
TP _{ILH}	Input rising delay	0.61 (0.8pF)	0.72 (2.4pF)	0.92 (4.8pF)	ns
TP_IHL	Input falling delay	0.88 (0.8pF)	1.03 (2.4pF)	1.24 (4.8pF)	ns
TP _{OLH}	Output rising delay	2.40 (10pF)	2.768 (30pF)	4.88 (60pF)	ns
TP _{OHL}	Output falling delay	1.905 (10pF)	2.614 (30pF)	5.03 (60pF)	ns
TR	Output rising time	1.052 (10pF)	2.761 (30pF)	7.83 (60pF)	ns
TF	Output falling time	0.932 (10pF)	2.133 (30pF)	6.23 (60pF)	ns





8. Package Information

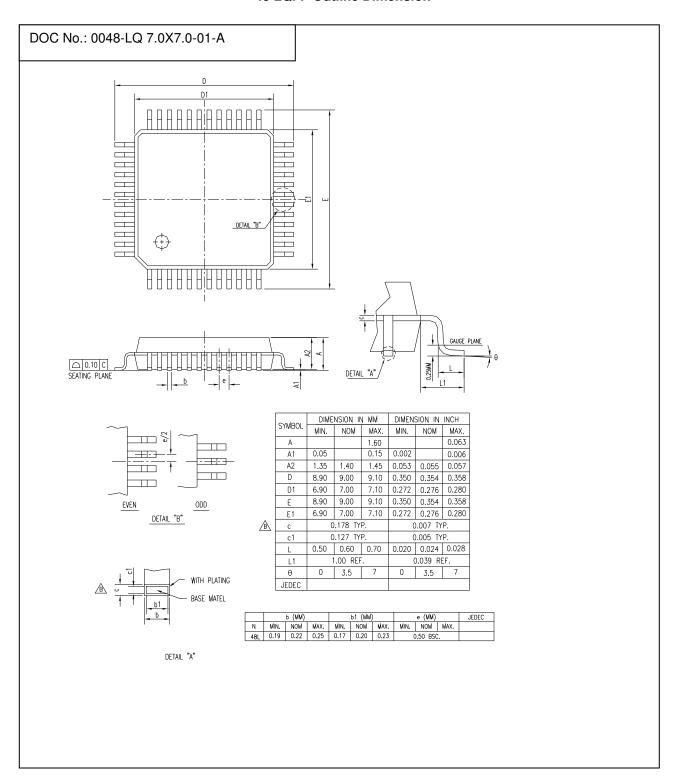
64 LQFP Outline Dimension



64 Pin LQFP 7.0x7.0x1.4 mm Package Outline Dimension



48 LQFP Outline Dimension









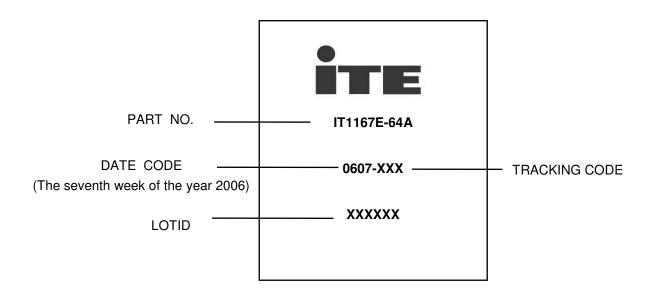
9. Ordering Information

Part No.	Package
IT1167E-64B/BX	LQFP 64
IT1167E-48B/BX	LQFP 48





10. Top Marking Information



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- Seller reserves the right to change credit terms at any time in its sole discretion.

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- Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).
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10. ENTIRE AGREEMENT

- (a) These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in written and signed by an officer of Seller.
- Buyer is not relying upon any warranty or representation except for those specifically stated here

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

JURISDICTION AND VENUE

The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.